IN THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1(Original). An arrangement for providing a reduced harmonic content output signal that represents a value of a digital input signal, the arrangement comprising:

plural storage devices configured to sample and store the digital input signal at different respective phases of a clock signal;

plural current steering digital-to-analog converters (DACs) configured to receive respective stored digital signals from respective ones of the plural storage devices, and to provide respective currents that represent the received stored digital signals; and

a combining arrangement configured to combine the currents from respective ones of the plural current steering DACs, so as to provide the reduced harmonic content output signal that represents the value of the digital input signal.

2(Original). The arrangement of Claim 1, wherein:

there are exactly two current steering DACs.

3(Original). The arrangement of Claim 2, wherein:

the plural storage devices store the digital input signal at two phases of the clock signal that are substantially 180° apart.

4(Original). The arrangement of Claim 1, wherein:

the plural storage devices store the digital input signal at N phases of the clock signal; and

$N > 2$.

5(Original). The arrangement of Claim 4, wherein:

the N phases of the clock signal are substantially equally spaced apart in phase, at substantially $(360/N)°$ apart.

6(Original). The arrangement of Claim 5, wherein:

there are exactly *N* current steering DACs.

7(Original). The arrangement of Claim 4, wherein:

there are exactly *N* current steering DACs.

8(Original). The arrangement of Claim 1, wherein:

the current steering DACs are configured to received the stored digital signal from the plural storage devices substantially continually, including periods between the phases of the clock signal at which the plural storage devices store the digital input signal.

9(Original). The arrangement of Claim 1, wherein the combining arrangement includes:

a set of electrical connections joining corresponding current outputs of the plural current steering DACs.

10(Currently Amended). The arrangement of Claim 1, wherein:

the plural current steering DACs and the combining arrangement ~~collectively~~ are configured to perform a low pass filtering function that causes the reduced harmonic content output signal to more closely approximate a sinusoidal signal.

11. Canceled.

12. Canceled.

13(Previously Presented). The arrangement of Claim 1, wherein:

the combining arrangement passes the reduced harmonic content output signal to a modulator without any intervening low pass filter.

14(Original). A transmission system including the arrangement of Claim 1.

15(Original). A transmission system including the arrangement of Claim 3.

16(Original). A transmission system including the arrangement of Claim 4.

17(Original). A method for providing a reduced harmonic content output signal that represents a value of a digital input signal, the method comprising:

sampling and storing the digital input signal at plural respective phases of a clock signal;

receiving respective stored digital signals stored in the storing step, and providing respective currents that represent the received stored digital signals; and

combining the currents so as to provide the reduced harmonic content output signal that represents the value of the digital input signal.

18(Original). The method of Claim 17, wherein the sampling and storing step includes:

sampling and storing the digital input signal at N clock signal phases that are substantially evenly distributed in phase.

19(Original). The method of Claim 18, wherein: $N>2$.

20(Original). A circuit configured to perform the method of Claim 17.